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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,519	08/28/2003	Ruthie D. Lyle	RPS920020141US1	6805

25299 7590 02/21/2007

IBM CORPORATION
PO BOX 12195
DEPT YXSA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER	
LUGO, DAVID B	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,519	LYLE ET AL.	
	Examiner	Art Unit	
	David B. Lugo	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 3, 9 and 10 are objected to because of the following informalities

a. Claim 2, recites "the first" [network] in line 2, however, a "first network" is not previously recited in the claim.

b. Claim 9, recites "the first" [network] in line 2, however, a "first network" is not previously recited in the claim.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-15 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3-8 and 11-17 of copending Application No. 10/650,385 in view of Miller et al. U.S. Patent 7,079,812.

Regarding claim 1, claim 1 of the '385 application discloses all of the limitations recited in claim 1 of the instant application, except that the interference detector and hop sequencer are formed on a substrate. Miller discloses a processor 140 in a transceiver 30 in Figure 5 which is coupled to coupled elements in physical engine 120 which are described as being used to determine signals from interfering networks (col. 4, line 50 to col. 5, line 15), and are located on a single chip (col. 5, lines 11-15). It would have been obvious to one of ordinary skill in the art to implement the various components of the apparatus of Panasik on a single substrate as disclosed by Miller in order to conserve space.

Further, claim 1 of the '385 application include limitations regarding a processor coupled to a memory which stores code for execution on the processor and which stores network transferable data, where the interference detector and the hop sequencer are coupled to the processor, and the stored network transferable data is transferable over the network, which are not recited in claim 1 of the instant application. It would have been obvious to one of ordinary skill in the art to remove those limitations along with their associated functionalities.

Regarding claims 2-7 of the instant application, see claims 3-8 of the '385 application, respectively.

Regarding claims 8 and 15, claim 11 of the '385 application discloses all of the limitations recited in claims 8 and 15 of the instant application, except that the mode switch, interference detector, and hop sequencer are formed on a substrate. Miller discloses a processor 140 in a transceiver 30 in Figure 5 which is coupled to coupled elements in physical engine 120 which are described as being used to determine signals from interfering networks (col. 4, line 50 to col. 5, line 15), and are located on a single chip (col. 5, lines 11-15). It would have been

obvious to one of ordinary skill in the art to implement the various components of the apparatus of Panasik on a single substrate as disclosed by Miller in order to conserve space.

Regarding claims 9-14 of the instant application, see claims 12-17 of the '385 application, respectively.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panasik et al. U.S. Patent 6,643,278 in view of Miller et al.

Regarding claim 1, Panasik discloses an apparatus in Figure 3 comprising an interference detector (physical engine 44) that detects interference from an interfering network as physical engine 44 is described as performing steps 16-24 of method 10 of Figure 2 (col. 12, lines 36-40) including detecting interference from an interfering network (step 22) and determining interfering hop sequence data relating to the interfering network (step 24) (see Fig. 2; col. 12, lines 58-62; col. 8, lines 21-52), where Panasik describes that the interfering network may be a FHSS network using a predetermined number of FHSS channels for frequency hopping (col. 10, lines 7-12), and the apparatus further comprises a hop sequencer (MAC controller 46) coupled to the interference detector which alters the hop sequence of a second FHSS network based on the interfering hop sequence data (see Fig. 2, steps 30, 32; col. 13, lines 6-9; col. 11, lines 1-38),

where the altered hop sequence comprises the same number of channels as the predetermined number of channels since the interfering (incumbent) network and the second (newly-entering) network may both be Bluetooth compliant networks (see col. 10, lines 7-12; col. 13, lines 31-34), thus having the same number of predetermined channels.

Panasik does not disclose that the interference detector and hop sequencer are formed on a substrate or chip. Miller discloses a processor 140 in a transceiver 30 in Figure 5 which is coupled to coupled elements in physical engine 120 which are described as being used to determine interferers from networks including interfering Bluetooth networks (col. 4, line 50 to col. 5, line 15), and are located on a single chip (col. 5, lines 11-15). It would have been obvious to one of ordinary skill in the art to implement the various components of the apparatus of Panasik on a single substrate as disclosed by Miller in order to conserve space.

Regarding claim 2, Panasik discloses that the altered hop sequence is a sequence which reduces the frequency of collisions between the networks (col. 6, lines 45-53).

Regarding claim 3, Panasik discloses that the altered hop sequence is the hop sequence of the interfering network having a predetermined translation applied thereto (col. 11, lines 4-7, 53-56).

Regarding claim 4, the altered hop sequence is an offset altered sequence (col. 11, lines 53-59).

Regarding claim 5, Panasik discloses in Figure 2 that the hop sequence of the second network is created and modified in steps 30-32, and where an offset is applied thereto in step 38.

Regarding claim 6, Panasik discloses that the offset altered sequence is the hop sequence of the interfering network having an offset applied thereto (col. 11, lines 4-7, 53-56).

Regarding claim 7, Panasik does not disclose that the interference detector detects interference as a degradation in network performance. Miller discloses a system for interference mitigation where traffic statistics indicating degradation in network performance is accumulated and used to detect interference (col. 5, lines 16-30). It would have been obvious to one of ordinary skill in the art to use information regarding degradation in network performance to detect interference as disclosed by Miller, in the system of Panasik because it enables interference detection without continuously searching for interferers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

David B. Lugo

David B. Lugo
Patent Examiner

2/16/07